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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,734	12/30/2003	Ken Nakahara	88519.0001	7543

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HOGAN & HARTSON L.L.P.
1999 AVENUE OF THE STARS
SUITE 1400
LOS ANGELES, CA 90067

EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
3663	

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07/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/748,734	NAKAHARA, KEN	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-6,8-11,13-15 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-6,8-11,13-15 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/11/07 has been entered.

Response to Amendment

Amendment filed with said Request for Continued Examination forms the basis for this Office Action. In said Amendment Applicant substantially amended claims 4-6 and 8-11. Claims 13-15 and 17-19 are also pending. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. ***Claims 4-6 and 8-11*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Specifically, the limitation "the electrode is disposed on a semiconductor device" is not supported by the Specification as originally filed including original claims. On the contrary, although the Specification does not explicitly disclose a semiconductor device through numeral, and only recite a "semiconductor light emitting device to which applicant's invention is applied" (see Figure legends and first paragraphs of the disclosure of Embodiments 1 and 2), - and hence a meaning conventional in the art needs to be understood, the meaning of semiconductor light emitting device includes both anode and cathode electrodes. Therefore, the claimed electrode as disclosed is part of said semiconductor light emitting device, which is quite different than being "disposed on it".

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. ***Claims 4-6 and 8-11*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, because "semiconductor device" has not been explicitly disclosed while a statement in the instant claim language places the electrode being disposed on a semiconductor device while for those of ordinary skill in the semiconductor device art the electrode is quite conventionally considered to be part of the semiconductor light emitting device referred to by applicant in his Specification, the meets and bounds of the limitation "electrode disposed on a semiconductor device" are not definite.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claim 4, 6, 10, 11, 13-15 and 19*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota (US 2002/0126719 A1) in view of Ishizaki (WO 02/89223) (national stage Ishizaki (US 2005/0224825 A1) serves in this office action as translation) (all as previously cited). This rejection is provided subject to the noted indefiniteness under 35 USC 112, second paragraph, under the assumption that "semiconductor device" means in the instant application the active (light-emitting) layer 22 sandwiched between n- and p- type GaN layers 21 and 23 of the semiconductor light-emitting device.

Kadota teaches a transparent electrode 43/49 (including a ZnO layer 43 (Figure 4, title, abstract, pages 1-3, especially [0035]-[0038]) (N.B.: ZnO is inherently transparent to light, as admitted by applicant in his specification) (N.B.: said ZnO layer is a low resistivity layer and abuts electrode 49 (Figure 4 and [0035], and hence qualifies as a component or extension of electrode 49);

wherein the electrode is formed on a a "semiconductor device" in the sense of applicant, namely disposed on 45/46/47 ([0035]).

Kadota does not necessarily teach the limitation "an Mg-doped ZnO film formed on the ZnO layer" as recited in claim 4.

However, it would have been obvious to include said limitation in view of *Ishizaki*, who, in a patent document on a production method for a light-emitting element, hence analogous art, teaches the application of MgZnO as buffer layer abutting sapphire substrate. It would have been obvious to insert a MgZnO layer between the ZnO layer and the sapphire layer in Kadota because the lattice constant of ZnO is 5.19 A (Table 5.5 in Wasa et al), that of (c-plane) sapphire is 4.76 A (see, e.g., Murakami, col. 5, l. 4-6) , of GaN 5.12. A (Sze), while that of MgO is less than that of ZnO (cf. Narayan et al, col. 10, l. 35-42), and hence doping with Mg of ZnO enables improved matching of the lattice constants of sapphire and ZnO through a buffer layer. *Motivation* to include the teaching by Ishizaki in the invention stems from the goal of Kadota to have buffer action between the members of the stack and the sapphire substrate: in fact, layer 43 is not only a low-resistivity layer abutting electrode 49 (and hence comprised in said electrode), it is also explicitly a buffer layer between the GaN stack and the c-plane sapphire layer ([0035]). However, as shown from the values of the lattice constants of GaN, ZnO and c-plane sapphire the buffer is not perfect and can be improved by inserting an Mg-doped ZnO layer, i.e., a MgZnO layer, between the ZnO buffer layer and the sapphire substrate that acts as a buffer between the ZnO buffer and the sapphire substrate, further improving lattice matching. *Motivation* to include the teaching by Ishizaki in the invention by Kadota derives from the further improvement of lattice matching. The examiner takes official notice that lattice matching improves light

efficiency. *Combination* of the teaching of a MgZnO buffer layer abutting the sapphire substrate merely requires the insertion of a layer in a layer stack and achieves meeting the claim because the Mg-doped ZnO layer is located on the ZnO layer when the positive vertical once and for all is defined to point down, while in the same coordinate system the ZnO layer is located on said semiconductor substrate. It is finally noted that a replacement of the ZnO buffer layer with a MgZnO buffer layer would not necessarily achieve the same improvement because the lattice mismatch at the interface with the GaN semiconductor layer would deteriorate.

Finally, it is noted that the wording "formed" (lines 4, 5) has patentable weight only in as much as "formed" can be replaced by "located": The limitation "formed" is only of patentable weight in as much as the method steps of formation distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

On claim 5: Kadota teaches an electrode structure comprising:

a transparent electrode 43/49 including ZnO (through 43) (note that ZnO is inherently transparent while this ZnO is low in resistivity (see [0035]); wherein the electrode is disposed on a semiconductor device 45/46/47 ([0035]-[0038]), and the semiconductor device includes GaN (through 45 and 47; loc.cit.).

Kadota does not necessarily teach an Mg-doped ZnO film formed on the electrode.

However, it would have been obvious to include said limitation in view of *Ishizaki*, who, in a patent document on a production method for a light-emitting element, hence analogous art, teaches the application of MgZnO as buffer layer abutting sapphire substrate. It would have been obvious to insert a MgZnO layer between the ZnO layer and the sapphire layer in Kadota because the lattice constant of ZnO is 5.19 A (Table 5.5 in Wasa et al), that of (c-plane) sapphire is 4.76 A (see, e.g., Murakami, col. 5, l. 4-6) , of GaN 5.12. A (Sze), while that of MgO is less than that of ZnO (cf. Narayan et al, col. 10, l. 35-42), and hence doping with Mg of ZnO enables improved matching of the lattice constants of sapphire and ZnO through a buffer layer. *Motivation* to include the teaching by Ishizaki in the invention stems from the goal of Kadota to have buffer action between the members of the stack and the sapphire substrate: in fact, layer 43 is not only a low-resistivity layer abutting electrode 49 (and hence comprised in said electrode), it is also explicitly a buffer layer between the GaN stack and the c-plane sapphire layer ([0035]). However, as shown from the values of the lattice constants of GaN, ZnO and c-plane sapphire the buffer is not perfect and can be improved by inserting an Mg-doped ZnO layer, i.e., a MgZnO layer, between the ZnO buffer layer

and the sapphire substrate that acts as a buffer between the ZnO buffer and the sapphire substrate, further improving lattice matching. *Motivation* to include the teaching by Ishizaki in the invention by Kadota derives from the further improvement of lattice matching. The examiner takes official notice that lattice matching improves light efficiency. *Combination* of the teaching of a MgZnO buffer layer abutting the sapphire substrate merely requires the insertion of a layer in a layer stack and achieves meeting the claim because the Mg-doped ZnO layer is located on the ZnO layer when the positive vertical once and for all is defined to point down, while in the same coordinate system the ZnO layer is located on said semiconductor substrate. It is finally noted that a replacement of the ZnO buffer layer with a MgZnO buffer layer would not necessarily achieve the same improvement because the lattice mismatch at the interface with the GaN semiconductor layer would deteriorate.

Finally, it is noted that the wording "formed" (lines 4, 5) has patentable weight only in as much as "formed" can be replaced by "located": The limitation "formed" is only of patentable weight in as much as the method steps of formation distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the

process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

On claim 6: the Mg-doped ZnO film of the combined invention is located to overlie an upper layer of the ZnO layer (namely: the Mg-doped layer is in between the sapphire substrate and the ZnO buffer layer (Figure 4), keeping in mind the definition of the positive vertical axis as pointing down, as defined in the discussion of claim 4.

On claim 10: the Mg-doped ZnO film 7 covers a portion of a side surface of the electrode. The latter would otherwise be more exposed to the environment. Therefore, the Mg-doped ZnO film 7 has the *capacity* to improve acid resistance of the transparent electrode. Furthermore, in reference to the claim language referring to "improves acid resistance of the transparent electrode", intended use, in this case the use as a protection against acids, and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

On claim 11: the semiconductor layer 47/46/45 is located on a substrate (e.g., 48 or 50 or 48/50) ([0035]-[0036]).

On claim 13: in the combined invention discussed under claim 4 the discussion of which is included herein by reference, the light-emitting device comprises a semiconductor layer 47/46/45 formed on a substrate (48 or 50 or 48/50; a ZnO

transparent electrode 43 formed on the semiconductor layer (again the same coordinate system is included wherein the positive vertical points down), and a Mg-doped ZnO film formed on the ZnO transparent electrode, wherein the semiconductor layer comprises a GaN system semiconductor layer 48/47/46/45/44 (or any single one of 44, 45, 46, 47, an 48).

On claim 14: in the combined invention discussed under claim 4 the discussion of which is included herein by reference, the light-emitting device comprises a semiconductor layer 48/47/46/45/44 formed on a substrate 50; a ZnO transparent electrode 43 formed on the semiconductor layer (again the same coordinate system is included wherein the positive vertical points down), and a Mg-doped ZnO film formed on the ZnO transparent electrode, wherein the semiconductor layer comprises a GaN system semiconductor layer 48/47/46/45/44 (or any single one of 44, 45, 46, 47, an 48).

Furthermore, the semiconductor layer comprises an p-type GaN system semiconductor layer 48 formed on a substrate 50, an emission layer 46 formed on the n-type GaN system semiconductor layer, and a n-type GaN system semiconductor layer (44, 45 or 44/45) formed on the emission layer (cf. [0035]-[0036] and Figure 4).

On claim 15: the Mg-doped ZnO film of the combined invention is located to overlie an upper layer of the ZnO layer (namely: the Mg-doped layer is in between the sapphire substrate and the ZnO buffer layer (Figure 4), keeping in mind the definition of the positive vertical axis as pointing down, as defined in the discussion of claim 4.

On claim 19: the Mg-doped ZnO film 7 covers a portion of a side surface of the electrode. The latter would otherwise be more exposed to the environment. Therefore,

the Mg-doped ZnO film 7 has the *capacity* to improve acid resistance of the transparent electrode. Furthermore, in reference to the claim language referring to "improves acid resistance of the transparent electrode", intended use, in this case the use as a protection against acids, and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

2. ***Claims 8-9 and 17-18*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota and Ishizaki as applied to claim 13 above, and further in view of Gibb et al (6,787,435 B2). All were previously cited.

As detailed above, claims 4 and 13 are unpatentable over Kadota in view of Ishizaki. *Neither Kadota nor Ishizaki necessarily teach* the further limitation defined by claims 8-9 or 17-18. *However, it would have been obvious to include said further limitations in view of Gibb et al, who, in a patent on a GaN system semiconductor layer based light-emitting device, hence analogous art,* teach a first metal pattern (metal stack 40))[0041]) for providing backside metallization and second metal pattern (solder pattern 44 ([0029]) to be formed on the semiconductor layer (same coordinate system is again adopted, with positive vertical coordinate increasing downward) so as to provide a suitable surface for providing heat sink or lead frame support. *Motivation* to include the

teaching by Gibb et al stems directly from said teaching by Gibb et al of the backside metallization and solder pattern for support.

Response to Arguments

Applicant's arguments filed 6/11/07 have been fully considered but they are not persuasive.

In response to Applicant's statements on page 7, final paragraph, of Remarks please be referred to the rejection of claim 4 herewith included by reference in its entirety.

In response to Applicant's traverse in the first paragraph of page 8, reference is made to par. [0037] in Kadota wherein the low resistivity properties of the ZnO are disclosed to be instrumental in enabling a current between electrodes 43 and 48/50. It needs to be realized that in addition to ZnO and Mg impurities abound in said ZnO layer, rendering its resistivity in a range that has zero as a limit point (see par. [0037]).

In response to Applicant's traverse on page 9, fourth paragraph, that the upper electrode is not acceptable as "substrate", examiner disagrees but, even arguendo, electrode is disposed on 48/50, which undoubtedly qualifies as a substrate. An alternative meaning of "substrate" as indicated by Applicant does not absolve examiner from giving "substrate" its broadest possible interpretation.

Comments in traverse of the rejections of the independent claims appear to fully rely on those provided for the independent claims.

Therefore, the instant claim language is rejected under the same art as cited previously.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
July 9, 2007

Primary Patent Examiner:

Johannes Mondt (TC3600, Art Unit: 3663)